

Spring 2011
ESE 311: Analog Integrated Circuits

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Office Hours: Monday, Wednesday, 4:30 - 6:30 PM, 247 Lt. Eng. bldg.
[Http://www.ece.sunysb.edu/~dima/ece311.html](http://www.ece.sunysb.edu/~dima/ece311.html)

Prerequisite: ESE372, Electronics

Course description: Engineering design concepts applied to electronic circuits; basic network concepts, computational analysis and design techniques; models of electronic devices; biasing and compensation methods; operational amplifiers designed by conventional and computer-aided techniques.

Lectures: Stony Brook Union 237, Monday, Wednesday, 2:20 - 3:40 PM

Textbook (required): Sedra, Smith, "Microelectronic Circuits", 6th ed., Oxford, 2010, ISBN 978-0-19-532303-0

Additional reading (recommended): Gray, Hurst, Lewis, Meyer, "Analysis and design of analog integrated circuits", 4th ed., Wiley, 2001, ISBN 0-471-32168-0

Grading: Homeworks (11%), Quizzes (9%), Project (15%), [Portfolio](#) (5%), Midterm 1 (15%), Midterm 2 (20%), Final exam (25%)

Topical outline:

<i>1. Single-ended IC amplifiers</i>	IC biasing, frequency response, active load, Miller's theorem, cascode amplifier	30%
<i>2. Differential amplifiers</i>	Differential pairs with active load, CM gain and CMRR, non-ideal characteristics, frequency response	30%
<i>3. Feedback and OpAmps</i>	Four basic feedback topologies, loop gain, stability and pole location, frequency compensation Two-stage OpAmp, folded cascode, OpAmp architectures	40%

Tentative schedule:

Mondays HW due	Wednesdays Quizzes	Topics	Textbook reading
Lect. 1 1/31	Lect. 2 2/2	IC fabrication technology. MOSFET and BJT characteristics. Cascode Amplifier. Current Mirrors.	Ch. 7, pp. 493-546, Appendixes 7A, B
Lect. 3 2/7, HW1	Lect.4 2/9, Quiz 1	CC-CE, CD-CS, CD-CE, CC-CB, CD-CG configurations. Comparison of MOSFET and BJT.	Ch. 7, pp. 546-569
Lect. 5 2/14, HW2	Lect. 6 2/16, Quiz 2	Differential pair. Current source load. Common mode gain and CMRR.	Ch. 8, pp. 587-650
Lect. 7 2/21, HW3	Lect.8 2/23, Quiz 3	Active load. Two-stage OpAmp.	Ch. 8, pp. 651-666
Lect. 9 2/28, HW4	Test 1 3/2	Review	Chapters 7-8
Lect. 10 3/7	Lect. 11 3/9	Frequency response. Miller's Theorem. Open-circuit time constants.	Ch. 9, pp. 687-719
Lect. 12 3/14, HW5	Lect. 13 3/16, Quiz 4	Differential amplifiers with active load. CM gain and CMRR. Frequency response	Ch. 7, pp. 720-748
Lect. 14 3/21, HW6	Lect. 15 3/23, Quiz 5	Non-ideal characteristics of differential amplifiers	Ch. 7, pp. 720-748
Lect. 16 3/28, HW7	Test 2 3/30	Review	Chapter 7
Lect. 17 4/4	Lect. 18 4/6	Four basic feedback topologies	Ch. 8, pp. 791-830
Lect. 19 4/11, HW8	Lect. 20 4/13, Quiz 6	Loop gain, stability and pole location, frequency compensation	Ch. 8, pp. 831-854
Spring Break (4/18-4/24)			
Lect. 21 4/25, HW9	Lect. 22 4/27, Quiz 7	Two-stage CMOS OpAmp. Folded cascode CMOS OpAmp.	Ch. 9, pp. 872-889
Lect. 23 5/2, HW10	Lect. 24 5/4, Quiz 8	OpAmp DC and small-signal analysis, gain, frequency response and slew rate	Ch. 9, pp. 889-921
Lect.25 5/9, HW11	Lect. 26 5/11, Quiz 9	Selected OpAmp architectures	
Final Exam			